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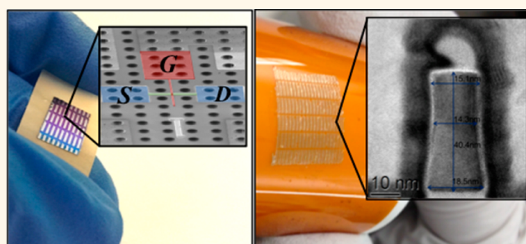
Nonplanar Nanoscale Fin Field Effect Transistors on Textile, Paper, Wood, Stone, and Vinyl *via* Soft Material-Enabled Double-Transfer Printing

Jhonathan P. Rojas,[†,§] Galo A. Torres Sevilla,[†,§] Nasir Alfaraj,[†] Mohamed T. Ghoneim,[†] Arwa T. Kutbee,[†] Ashvitha Sridharan,[‡] and Muhammad Mustafa Hussain*[,†]

[†]Integrated Nanotechnology Lab, King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia and [‡]The KAUST Schools, King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia. [§]These authors contributed equally to this work.

ABSTRACT The ability to incorporate rigid but high-performance nanoscale nonplanar complementary metal-oxide semiconductor (CMOS) electronics with curvilinear, irregular, or asymmetric shapes and surfaces is an arduous but timely challenge in enabling the production of wearable electronics with an *in situ* information-processing ability in the digital world. Therefore, we are demonstrating a soft-material enabled double-transfer-based process to integrate flexible, silicon-based, nanoscale, nonplanar, fin-shaped field effect transistors (FinFETs) and planar metal-oxide-semiconductor field effect transistors (MOSFETs) on various asymmetric surfaces to study their compatibility and enhanced applicability in various emerging fields. FinFET devices feature sub-20 nm dimensions and state-of-the-art, high-κ/metal gate stacks, showing no performance alteration after the transfer process. A further analysis of the transferred MOSFET devices, featuring 1 μm gate length, exhibits an I_{ON} value of nearly 70 μA/μm (V_{DS} = 2 V, V_{GS} = 2 V) and a low subthreshold swing of around 90 mV/dec, proving that a soft interfacial material can act both as a strong adhesion/interposing layer between devices and final substrate as well as a means to reduce strain, which ultimately helps maintain the device's performance with insignificant deterioration even at a high bending state.



KEYWORDS: double-transfer · soft material · nonplanar · FinFETs · asymmetric surface

Flexibility has become a key feature and game changer that allows not only large-scale deployment of electronics in what is now known as macro-electronics[1] but also offers the possibility of integration of electronics with wavy, curvilinear, irregular, or asymmetric shapes and surfaces, such as textile, paper, vinyl, wood, glass, stone, and tiles. This can leverage the development of electronic display, lighting, distributed sensor networks, large-surface energy harvesting (such as photovoltaic, thermoelectric generator, *etc.*), or biointegrated systems enabling the Internet of Everything.[2−8] In the recent past, the display industry has focused on making curved, large, flat-panel display screens. Organic and polymeric materials, as well as amorphous silicon (a-Si) and low-temperature poly-crystalline silicon (LTPS)-based electronics, have played an important role in the development of such display technologies.[9−11] Moving forward, the development of new and exciting flexible, stretchable, and wearable high-performance technologies is a critical enabler for the Internet of Everything.[1] Since continuous data transmission from various wearable electronics to the cloud is acutely energy inefficient, involving excessive power consumption through large-bandwidth wireless communication, centralized massive data processing, and because of potential cybersecurity issues due to hacking and technical vulnerability, it is important to integrate *in situ* data-processing capability and storage in wearable electronics for energy-efficient functionality and information management. In that regard, out of a wide variety of existing materials (organic, molecular, nanoparticles, quantum dots, nanowires, nanotubes, thin film, *etc.*), inorganic, thin film based electronics show the most reliable and

* Address correspondence to muhammadmustafa.hussain@kaust.edu.sa.

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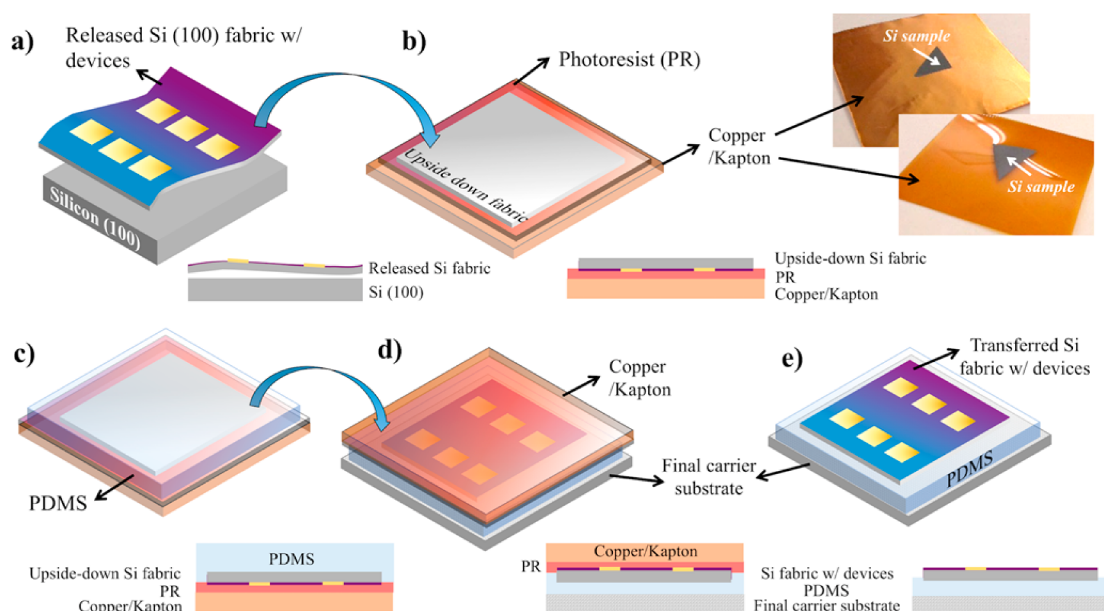


Figure 1. 3D and 2D schematics describing the fabrication process flow of the double-transfer process of silicon (100) fabric onto a variety of asymmetric surfaces.

effective high-performance information-processing capability. Some significant challenges with such electronics include their rigidity, and brittleness; therefore, it is essential to make them lightweight and flexible without compromising their advantages of higher information-processing ability, thermal stability, integration density, and energy efficiency (due to sub-1 V low-input operation). Their flexural rigidity can be reduced, and remarkable flexibility may be attained in making them ultrathin. Various methods[12−16] have been demonstrated with interesting applications, including two[18−23] of our own where we uniquely used the bulk monocrystalline silicon (100), which holds 90% of the electronics market share with prefabricated devices, retaining ultralarge-scale-integration (ULSI) density to demonstrate flexible, ultrahigh-performance, nanoscale, nonplanar FinFETs—semiconductor industry's most advanced transistor. While these methods are exciting, their nonplanar, nanoscale features pose a difficult challenge for integration with various asymmetric surfaces readily available in our daily life, including textile, paper, wood, stone, and vinyl. Not only do these materials have irregular curvilinear surfaces, but mitigating stress, while preserving structural integrity in their embodiment with flexible ultrathin layered materials with sensitive nanoscale featured devices, is demanding. Soft-materials can serve as both an interposing and an encapsulation layer. D.-H. Kim *et al.*, for example, demonstrated the transfer printing of ultrathin circuits on different materials and irregular surfaces.[17] In continuation of such pioneering work, we have now adapted a double-transfer technique onto soft materials with embedded, nanoscale, nonplanar, state-of-the-art FinFETs and MOSFETs on asymmetric surfaces of textile, paper, wood, stone, and vinyl as a prime example of how our digital world will take shape in the future after the heterogeneous integration of traditional but quite mature and reliable CMOS technology with up-and-coming, transfer techniques using soft materials as the prime enabling catalyst.

RESULTS AND DISCUSSIONS

The heterointegration process is shown in Figure 1. It begins with the release of a thin layer of silicon of about 30−35 μm in thickness from a *p*-type (100) silicon wafer (Figure 1a). The procedure of extracting such a fabric consists of deep trench formation followed by isotropic etching-based release, which has been demonstrated with various devices and thicknesses (5−50 μm) by controlling various design parameters, such as the trenches' depth, as explained in detail in our previous works.[25,26] The transfer process is then carried out by placing the released silicon fabric upside-down on a piece of polyimide film (Kapton) or copper foil, which is coated with unbaked photoresist (Figure 1b). The photoresist layer is meant to protect the topside of the fabric, where electronic devices "sit", and we have found that a thick layer is the most effective (above 2 μm). Once the photoresist is baked, a thin layer of elastomer polydimethylsiloxane (PDMS) is spin coated on top to provide final adhesion and isolation from applied strains (Figure 1c). The whole stack is then placed on top of the substrate of interest, and the PDMS layer is left for curing (Figure 1d). Finally, the photoresist is dissolved with acetone to release the carrier film/foil (Figure 1e). This double-transfer approach differentiates itself from the standard single-transfer and printing approach, which relies on the mechanical properties of nanomembranes with usually

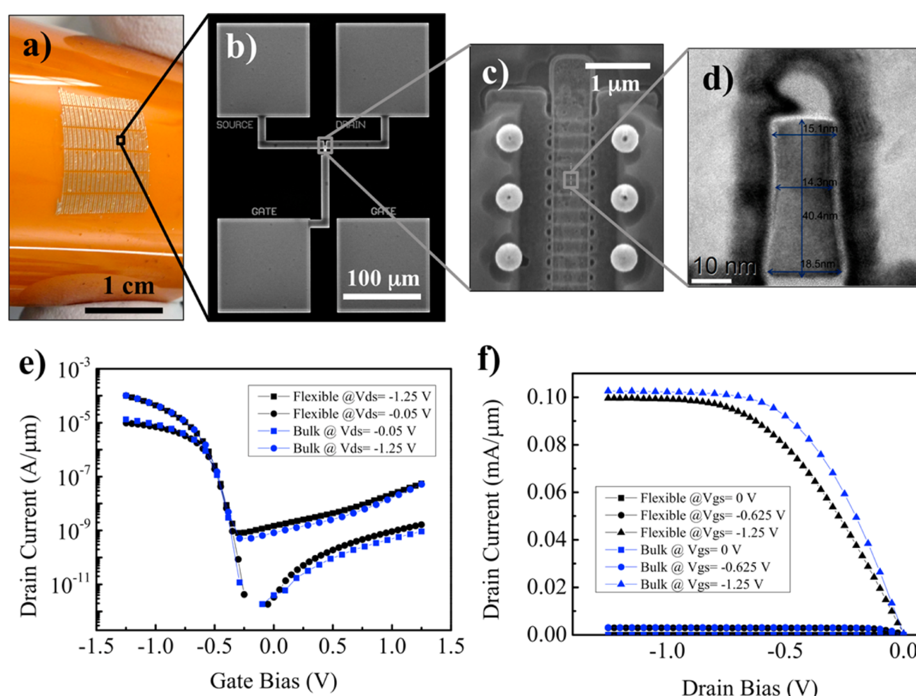


Figure 2. (a) Digital photograph of transferred FinFETs die. (b) Scanning electron microscope (SEM) image of a single FinFET device. (c) SEM zoomed-in image of the gate on top of fins. (d) Tunnel electron microscope (TEM) image of one fin with dimension. (e) Linear and saturation transfer *I*−*V* characteristics of a representative FinFET device (L = 1 μm, W = 3.6 μm) before and after thinning and transfer processes (absolute current values). (f) Output characteristics of a representative FinFET device before and after thinning and transfer processes (absolute current values).

very small areas for single-device development. In contrast, we offer the opportunity of large-area, complete-die transfer with ultralarge-scale density capability.

We have chosen PDMS over other materials because of its favorable mechanical and insulating properties as well as its biocompatibility demonstrated through its use in several implants, bandages, contact lenses, and a variety of other medical uses.[27] PDMS can be considered as a variety of silicone: inert, synthetic compounds whose basic structure is the inorganic compound of Si atoms with oxygen atoms (siloxane) and methyl groups occupying the remaining free valences. Moreover, it is inexpensive, transparent, and stretchable, and it can be conformably coated with a controlled thickness in addition to its capacity to form mold structures with high resolutions.

To demonstrate sophisticated nonplanar devices, we have fabricated and transferred *p*-type, state-of-the-art, 3D, nonplanar, double-gate FinFET with improved electrostatic control, featuring high-κ/metal gate materials and displaying exceptional electrical performance and reduced short-channel effects. Starting up with an 8-in. silicon-on-insulator (SOI) wafer, deep ultraviolet light (DUV) and resist trimming were used to pattern the fins and thus achieve features down to 20 nm. Next, a reactive ion etching (RIE) was used to anisotropically etch the silicon layer. Then, 20 nm of titanium nitride (TiN) and 4 nm of hafnium dioxide (HfO_2) formed the high-κ/metal gate stack, followed by 200 nm of polysilicon deposited by chemical vapor deposition (CVD). After gate patterning, ion implantation was used to form source and drain; ohmic contacts were then created with a silicidation process using nickel. Finally, aluminum contacts were formed and a forming gas (N_2/H_2) anneal was performed at 420 °C. Once fabricated, the wafer was diced and a die was selected for the soft back-etching process to thin the carrier substrate down to 50 μm. Details on the thinning process can be found in our previous publication.[24] Next, the thin die was transferred onto a Kapton plastic with the previously described procedure (Figure 2a). Figure 2b−d also displays scanning and tunnel electron microscopy (SEM and TEM) images with the detailed dimensions of the fins as well as the output and transfer current−voltage (*I*−*V*) characteristics (Figure 2e,f) of the fabricated device, comparing its behavior before and after the thinning and transfer processes were carried out. Table 1 shows the comparison of several important extracted parameters, which confirms there is only negligible change in performance once the transfer process is completed. In the past, we have performed a more comprehensive electrical study on how the mechanical motion of different bending radii (from 5 cm down to 0.5 cm) affects the main electrical characteristics of the FinFETs (including threshold voltage, subthreshold swing, effective mobility, transconductance, drain-induced barrier lowering (DIBL), and gate delay and leakage current).[24,28]

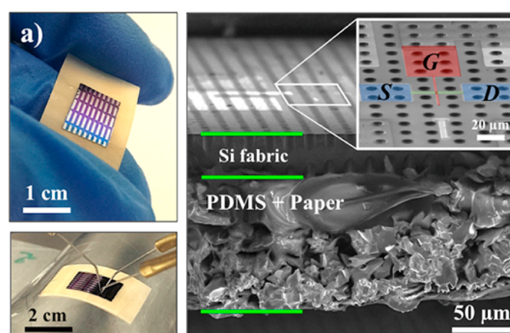
TABLE 1. Comparison of Important Extracted Characteristics of a FinFET Device before and after the Thinning and Transfer Processes Were Performed

	SS_{LIN}[a] [mV/dec]	SS_{SAT}[b] [mV/dec]	V_{TH_LIN}[a] [mV]	V_{TH_SAT}[b] [mV]	I_{ON}/I_{OFF} [Dec]	μ_{EFF} [cm^2/V·S]
As fabricated	−61	−65	−596	−501	3.3	−102
Transferred	−62	−63	−563	−518	3.25	−100
% Change	2%	−2%	−5%	3%	−1.5%	−2%

[a] Extracted from the linear region. [b] Extracted from the saturation region.

To further study the implications of the transfer process, we have additionally fabricated and characterized *n*-type planar traditional MOSFETs, as they are the dominant transistors in any advanced low-standby power (LSTP) and low-power (LOP) circuitry. We made them flexible and semitransparent through our trench-protect-release-reuse-based process and then transferred them onto paper (Figure 3a) with the purpose of examining the stress effect on the electrical behavior of the transistors. The fabrication process started with the active area's definition within a silicon dioxide insulating layer, and then a gate stack was formed on top. The gate stack consisted of a thin layer of silicon dioxide (20 nm SiO_2) grown with thermal oxidation and polycrystalline silicon (200 nm) and deposited with plasma-enhanced chemical vapor deposition (PECVD). Gate dimensions were patterned with photolithography and RIE to obtain features down to 1 μm (inset in Figure 4a). Silicon nitride spacers were formed to protect the gate stack. Next, source and drain areas were created with ion implantation at the gate's sides. Nickel silicidation was then performed to improve contact resistance, and finally aluminum contacts (200 nm-thick) were deposited with sputtering and then patterned with RIE. Next, before carrying out the releasing process, the top exposed silicon and polysilicon areas were protected with a thin layer of Al_2O_3 deposited with atomic layer deposition (ALD). The peel-off process was then performed as previously described to separate a thin top layer (2 cm × 1 cm × ~40 μm) from the substrate with the devices on top. Finally, the transfer process was carried out on a piece of paper with the method explained previously.

Stress can play an important role in determining the transistor's behavior, and one of the key mechanisms in silicon is the piezoresistive effect, by which the bulk resistivity is influenced by the mechanical stress applied to the material and how it is applied. From a physical structure point of view, stress directly affects the bandgap distribution, which causes changes in the effective mass of carriers. For electrons, stress causes redistribution in the sub-bands, whereas, for holes, stress causes band split and deformation. Given that mobility depends on the effective mass of carriers, stress can directly affect device performance.[29,30] On the other hand, only a small performance reduction



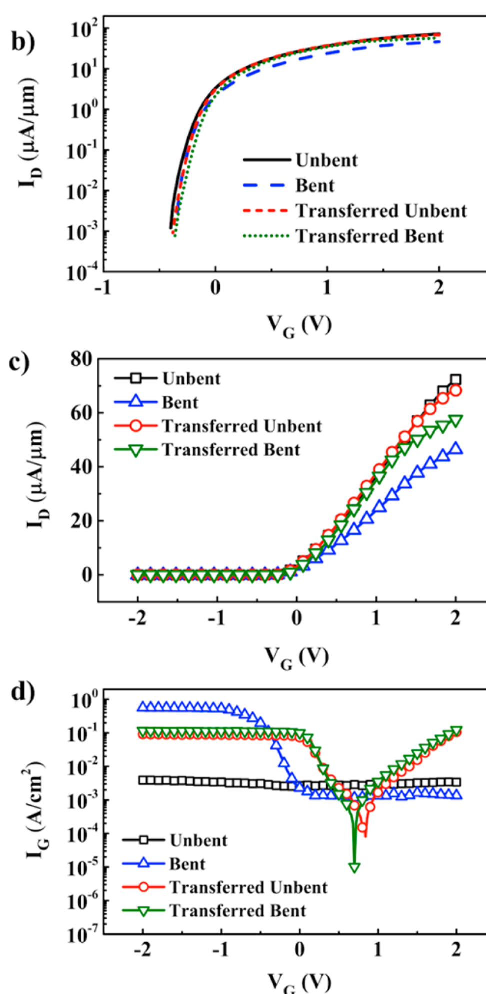


Figure 3. (a) Digital photographs and scanning electron microscope (SEM) images of *n*-type MOSFET devices on a 40-μm-thick silicon fabric knitted on paper. (b and c) Subthreshold and saturation *I*−*V* characteristics of representative MOSFET device (*L* = 1 μm, *W* = 10 μm) during different measurement stages. (d) Gate leakage current density at different measurement stages (V_{DS} = 2 V in all graphs).

was observed in MOSFET devices after our CMOS-compatible peel-off process was performed, compared with the on-wafer devices (where the most significant impact is on gate leakage current) and at different applied strains (bending radii from 70 mm down to 5 mm or approximately 0.2% strain).[21] Here, we have transferred a flexible silicon fabric with MOSFET devices and characterized their performance before the

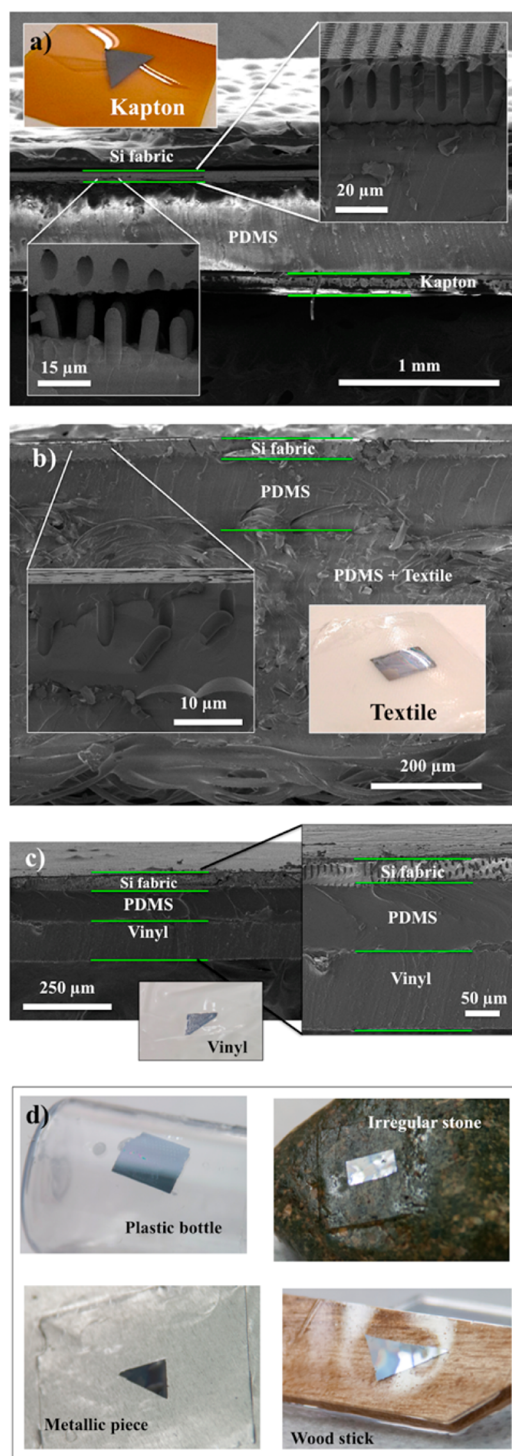


Figure 4. Scanning electron microscope (SEM) images and optical images of released silicon sheets on (a) polyamide (Kapton), (b) textile, and (c) vinyl glove. (Insets in SEMs show zoomed-in versions and in (a) and (b), the formation of polymeric pillars formed during PDMS curing through the fabric's holes for increased grasp.) (d) Digital photographs of flexible silicon sheets transferred onto more complex, extremely irregularly surfaced objects, such as a plastic bottle, metal, stone, and wood.

transfer (flat and bent to a radius of 3.5 mm) and after the transfer (flat and bent to a radius of 3.5 mm; bending occurs in a longitudinal direction across the device channel). Figure 3b,c shows the $I-V$ characteristics in the subthreshold and linear regions as well as leakage current density. As can be observed, before the silicon fabric is transferred, bending causes a noticeable detriment regarding on-state and gate leakage currents. We have previously shown that flexibility can cause some electrical degradation in ultrathin flexible fabrics due to continuous mechanical stress, which is reflected in a high-capacitance variation and increased interface defect density in the dielectric.[31] It has been previously demonstrated that the presence of defects in the dielectric leads to a higher trap-assisted tunneling current, which at the same time produces an increment in leakage current.[32,33] But once our transfer process was performed, the impact of bending was nearly eliminated when compared with the bare silicon fabric, which can be explained by the strain reduction effect with the addition of the soft polymeric material. Table 2 summarizes the changes of important electrical parameters in the MOSFET device, and it is evident that, after the transfer process, the device not only retained its functionality with tolerable variations, but also recovered its performance and reduced strain-related effects, with the additional observation that remaining defects in the dielectric will still affect the gate leakage current, as observed in Figure 3d.

Regarding the mechanical characteristics of the transferred samples, we first observed that different adhesion mechanisms were involved at the Si/PDMS and PDMS/substrate interfaces. In the Si/PDMS interface, adhesion was promoted through trapping of the Si sheet inside the cured PDMS. Figure 4a–c shows scanning electron microscopy (SEM) images of silicon fabrics (~30 μm in thickness) on top of the Kapton, textile, and vinyl, showing how the PDMS penetrated up to the holes for better grip. But we also observed that the penetration rate of PDMS into the substrate material increased rapidly when the porosity of the substrate was increased. Textile (Figure 4b) and wood (Figure 4d) substrate materials exhibited strong adhesion to the Si sheet when compared with less porous surfaces, such as Kapton or vinyl (Figure 4a,c). Thus, using PDMS was expected to work for other materials because it provided an adhesion route independent of the chemistry at both interfaces of Si/PDMS and PDMS/substrate. At the same time, because of the strong adhesion, the main failure mechanism occurred from cracking at the ultimate tensile strength of the fabric, rather than slipping or delamination, which have been found to be a more common failure for relatively larger silicon thicknesses.[14]

Not only limited to adhesion promotion, the low modulus PDMS layer reduced the applied strain on the silicon fabric. To appreciate this, the concept of mechanical neutral surfaces must be considered. According to Suo *et al.* for materials with quite large differences in the elastic moduli, the neutral surface between a Si sheet

TABLE 2. Fabricated MOSFET Electrical Parameters at Different Stages and Their Relative Change Compared to Their Initial States

	I_{ON} [μA/μm][a]	[%]	I_{OFF} [mA/cm^2][b]	[dec][c]	V_{TH} [mV]	[%]	subthreshold swing [mV/dec]	[%]
Unbent	72.3	-	3.44	-	−158.5	-	87.83	-
Bent	46.4	−35.8	529	2.2	−166	4.9	91.23	3.9
Transferred Unbent	68.3	−5.5	87	1.4	−147	−7.2	89.85	2.3
Transferred Bent	57.5	−20.5	113	1.5	−130	−18	90.88	3.5

[a] Current at V_{DS} = 2 V, V_{GS} = 2 V. [b] Current density at V_{DS} = 2 V, V_{GS} = −1 V. [c] Difference in decades.

and an underneath compliant material must shift from the midsurface toward the compliant material.[34] Since PDMS has a low elastic modulus of 0.5 MPa compared to the large elastic modulus for silicon, the neutral surface must shift accordingly. Depending on the thicknesses of both the Si sheet t_{Si} and the PDMS t_{PDMS}, their corresponding Young's moduli Y_{Si} and Y_{PDMS}, and R, the bending radius, a reduction of the applied strain on the Si sheet is expected and governed by the relation:[34]

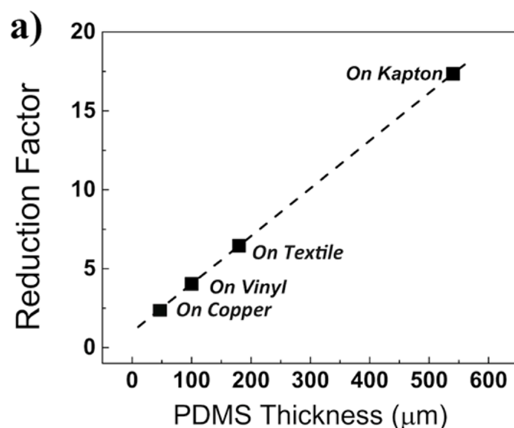
$$\epsilon_{top} = \frac{t_{Si} + t_{PDMS}}{2R} \frac{1 + 2\eta + \chi\eta^2}{(1+\eta)(1+\chi\eta)} \quad (1)$$

where $\eta = t_{Si}/t_{PDMS}$ and $\chi = Y_{Si}/Y_{PDMS}$. Thus, depending on the PDMS thickness it is possible to control the reduction factor, as illustrated in Figure 5a, for different PDMS thicknesses, achieving up to almost 20 times the strain reduction. This directly affects the tensile strength of the system and helps achieve lower-bending radii for more compliant fabrics. To illustrate this effect, we have compared the minimum bending radius of a released ~10 μm silicon fabric with a transferred sample with similar dimensions. For a PDMS thickness of around 50 μm, the sample achieved a bending radius as small as 1 mm (Figure 5b), compared to ~2 mm of the self-standing silicon fabric by itself.

On the other hand, adding a top encapsulating layer on the silicon sheet would not only act as protection from diverse environmental conditions but it can also be adjusted so that the neutral surface (where there is no strain) shifts to where the silicon substrate is bending so that it does not add any strain to the electronic devices. This condition is met when[34]

$$Y_{Si} t_{Si}^2 = Y_{encp} t_{encp}^2 \quad (2)$$

where Y_{encp} and t_{encp} are the young modulus and thickness of the encapsulating material. In the case of a 30-μm-thick released silicon fabric, this value is about 120, which corresponds to a PDMS thickness of approximately 15 μm. This same concept of mechanical improvement by shifting of the encapsulating layer and neutral surface has been previously studied by S.-I. Park *et al.*[14] Transforming thin-film-based, traditional, inorganic electronics by reducing their thickness is an effective way to achieve flexible electronics, and using a PDMS-based support layer can lead to an effective way for encapsulation of such electronics as a packaging layer.



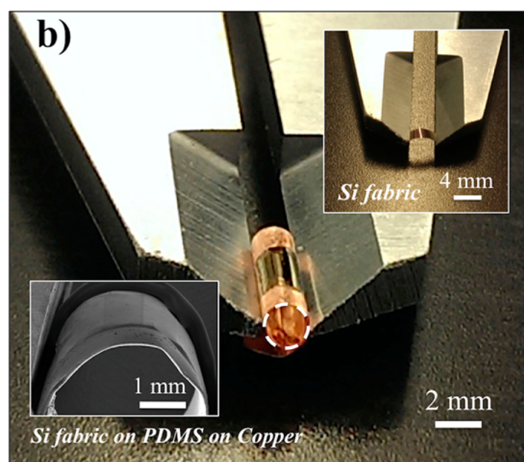


Figure 5. (a) Strain reduction factor due to the presence of a lower young modulus material (points were taken from the PDMS thicknesses from Figures 1a−c and 2b). (b) Digital photograph of a released silicon fabric on top of a 50-μm-thick PDMS layer coated on a copper foil. Insets show an SEM image of the bended fabric on PDMS/copper and the smaller bending radius attained with a self-standing silicon fabric of similar thickness and dimensions. Copper foil is widely used for graphene growth, and this work shows a pathway for heterointegration of CMOS circuitry with graphene-based radio frequency (RF) devices without any transfer of graphene layers, which is considered to be a challenging impediment.

CONCLUSIONS

We have shown a generic heterointegration of transfer printing and CMOS technology-derived, state-of-the-art logic devices with both nonplanar 3D FinFETs and planar traditional MOSFETs on thin flexible substrates and a highly flexible monocrystalline

silicon (100) fabric (derived from bulk substrate) to knit (weave) on various wavy, curvilinear, irregular, or asymmetric surfaces (such as textile, paper, stone, wood, vinyl, *etc.*) for wide deployment of high-performing, flexible electronics needed for information processing, data distribution in distributed sensor networks, and other large-surface-area, curvilinear electronic applications. The use of a soft polymeric material gives us a way to not only provide a strong adhesion layer to reduce the strain and achieve more compliant systems but also encapsulate ultra-thin, silicon fabric-based, flexible electronics. Overall, transferring the silicon fabric with devices not only facilitates handling and adds mechanical robustness but also helps reduce applied stress to devices, which ultimately helps maintain their functioning performance with insignificant deterioration even at a bending state.

METHODS

FinFET Fabrication and Thinning. The fabrication process began with an 8-in. silicon-on-insulator (SOI) wafer (90 nm silicon on top of 125 nm BOX). The fins (15−20 nm width) were first patterned through deep ultraviolet lithography (DUV) and resist trimming. Next, a high-κ/metal gate stack (4 nm of hafnium dioxide (HfO_2) and 20 nm of titanium nitride (TiN)) was formed through atomic layer deposition (ALD). Then, 200 nm of poly-silicon was deposited by chemical vapor deposition (CVD). A careful etching process was performed to pattern the gate stack with no residual; then silicon nitride (Si_3N_4) spacers were formed at each side of the gate. Next, to form the source and drain, ion implantation (boron (B) in the case of *p*-type doped silicon) was used, followed by activation annealing. Nickel silicidation (NiSi) was formed subsequently through deposition of 15 nm of Ni, followed by 10 nm of TiN, then annealed at 450 °C. Interlayer dielectric (ILD) was formed with phosphosilicate glass (PSG) and plasma-enhanced chemical vapor deposition (PECVD) silicon oxide (SiO_2). Next, contact holes were etched through the ILD, after which titanium (Ti) was deposited as a barrier layer, then tungsten as plugs, and finally aluminum (Al) as contact pads. Further details can be found in the corresponding author's previous work.[28−35] The thinning process can be summarized as the anisotropic back-etching of a selected die through several steps of deep reactive ion etching (DRIE) to adequately reach the desired thickness. A detailed description of this process can also be found in our previous work.[24]

MOSFET Fabrication. The fabrication started with lightly doped *p*-type 4-in. bulk Si wafers. First, 300 nm of SiO_2 was grown thermally using a dry-wet−dry oxidation process. Next, the wafers were spin coated with diluted nLof 2070 photoresist to perform the first lithography; the resist thickness due to dilution was coated to a thickness of 1 μm (speed, 4000 rpm for 30 s; bake, 5 min at 100 °C). Then, the exposure was performed with research-level contact aligner EVG6200 with a constant dose of 300 mJ/cm^2 and a postexposure bake was performed (1 min at 100 °C). Resist development was done for 1 min in a 726 MIF developer. At this point, the wafers were ready to perform the first etch step, which created the openings for the active area of the transistor. The first etch was divided in two: anisotropic reactive ion etching to remove the first 270 nm of SiO_2 (ICP power, 1500 W; RF power, 150 W; CHF_3, 40 sccm; O_2, 5 sccm; temperature, 10 °C; pressure, 10 mTorr), followed by wet etch in buffered oxide etchant (BOE) for 45 s to remove the remaining 30 nm of SiO_2 without damaging the Si surface. Next, the resist is removed in plasma asher (950 W of power; 100 sccm O_2; 14 sccm Ar; temperature, 120 °C; pressure, 500 mTorr). Then, the wafers were cleaned in Piranha, SC1 and DHF before the gate stack oxide growth. The gate oxide was grown thermally at 950 °C for 20 min of dry-oxidation to obtain a thickness of 20 nm. Then, poly-Si was deposited on top of the wafer (temperature, 650 °C; pressure, 1000 mTorr; SiH_4 flow, 50 sccm; Ar flow, 450 sccm; forward power, 10 W) for 5 min, obtaining a 200 nm-thick film. Next, the wafers went through a second lithography step following the same steps as the ones performed for active definition. In this step, the gate stack was defined and it was etched following two different steps: first, poly-Si was etched using dry etching (ICP power, 250 W; RF power, 100 W; temperature, 10 °C; pressure, 5 mTorr; HBr, 50 sccm; Cl_2, 20 sccm). Second, the gate oxide was removed with a timed wet BOE etch (30 s). Next, the resist was removed with the same process as was done in the first resist removal. Then, 50 nm of silicon nitride was deposited on top of the wafer (total time, 4 min; low frequency pulse time, 6 s at 0.3 MHz; high frequency pulse time, 14 s at 13.56 MHz; temperature, 300 °C; pressure, 850 mTorr; SiH_4 flow, 23 sccm; NH_3 flow, 20 sccm; N_2 flow, 980 sccm; forward power, 20 W). The silicon nitride was then etched using a combination of dry and wet etch to create the spacer; the first etch removed 45 nm of Si_3N_4 (ICP power, 1500 W; RF power, 100 W; CHF_3, 40 sccm; O_2, 5 sccm; temperature, 10 °C; pressure, 10 mTorr), and the remaining 5 nm were removed with buffered oxide etchant for 10 s. At this point, the wafers had the source and drain exposed and were ready to be implanted. The wafers were implanted with arsenic ions with the following conditions: dose = 4×10^{15} ions/cm^2 and energy = 20 keV. Then, the wafers were processed with vapor HF for 15 s to remove any native oxide. Next, 20 nm of Ni was deposited on top of the wafers and annealed for 30 s at 450 °C to create NiSi and eliminate contact resistance between the aluminum pads and the source, drain and gate contacts. The remaining nickel was then removed using Piranha. Next, 200 nm of Al were deposited on top of the wafers, and a third lithography process was performed using the same procedure as the first two lithography steps. At this point, the photoresist defined the contact pads and source, drain, and gate connections. Then, a combination of dry and wet etch was performed to define the aluminum pads and contacts; dry etch (temperature, 80 °C; *Step 1:* ICP power, 1500 W; RF power, 50 W; pressure, 40 mTorr; Cl_2, 10 sccm; BCl_3, 40 sccm; Ar, 10 sccm; *Step 2:* ICP power, 1500 W; RF power, 150 W; pressure, 20 mTorr; Cl_2, 40 sccm; BCl_3, 10 sccm; *Step 3:* ICP power, 1500 W; RF power, 50 W; pressure, 40 mTorr; Cl_2, 10 sccm; BCl_3, 30 sccm; Ar, 20 sccm; *Step 4:* RF power, 150 W; pressure, 900 mTorr; O_2, 100 sccm) was performed for 1 min to remove the first 150 nm of aluminum and 1 min of wet etch in standard Al etchant removed the remaining aluminum without damaging the silicon surface. Next, 40 nm of aluminum oxide was deposited with atomic layer deposition (TMA precursor time: 15 ms, $H_2O_{vapor:}$ 15 ms, 400 cycles at 250 °C) to protect the top silicon and poly-Si exposed surfaces. A fourth and final lithography step was then performed on the wafers using ECI 3027 photoresist (spin speed, 1750 rpm; bake, 1 min at 100 °C) to define the silicon etch holes. The wafers went through two different dry etch steps: the first one removed the 300 nm of SiO_2 from the etch holes (ICP power, 1500 W; RF power, 150 W; CHF_3, 40 sccm; O_2, 5 sccm; temperature, 10 °C; pressure, 10 mTorr), and the second created deep trenches (~45 μm) in the silicon wafer (90 cycles, temperature, −20 °C; etch step, 7 s; ICP power, 1300 W; RF power, 30 W; pressure, 35 mTorr; C_4F_8, 5 sccm; SF_6, 120 sccm; deposition step, 5 s; ICP power, 1300 W; RF power, 5 W; pressure, 35 mTorr; C_4F_8, 100 sccm; SF_6, 5 sccm). The wafer then went through a second 40 nm of aluminum oxide deposition using atomic layer deposition (TMA precursor time: 15 ms, $H_2O_{vapor:}$ 15 ms, 400 cycles at 250 °C), this time to protect the sidewalls of the trenches. At this point, the wafers were taken to a final dry etch step (ICP power, 1500 W; RF power, 150 W; CHF_3, 40 sccm; Ar, 5 sccm; temperature, 10 °C; pressure, 5 mTorr), where the trench sidewall spacers were created to protect the silicon from

the subsequent etch step and leave the bottom of the trenches exposed for the silicon release process. Finally, the wafers were taken to xenon difluoride (XeF_2) etchant, where caves were created at the bottom of each trench; once these caves converged, the top silicon portion containing the transistors was released from the bulk and could be flexed due to its extremely low thickness.

Electrical Characterization. A semiconductor parameter analyzer (Keithley 4200-SCS) and a probe station (Cascade) were used to obtain the $I-V$ characteristics. A metal plate with a predefined bending radius of 3.5 mm was used to evaluate the electrical performance of the MOSFET devices at a bent state (as shown in Figure 3a).

Transfer onto Asymmetric Surface. A piece of polyimide film or copper foil was coated with unbaked photoresist (PR) (MicroChemicals, 4 mL ECI 3027, 4 μm: 1750 rpm for 30 s). A released silicon fabric was then placed upside-down on top of the PR, which was then baked at 100 °C for 60 s. Polydimethylsiloxane (PDMS) was coated on top (No spin, ~1 mm thick; 500 rpm for 30 s, ~100 μm thick; 1750 rpm for 30 s, ~50 μm thick). The stack with uncured PDMS was positioned on top of the substrate of interest and it was then left for curing (24 h at room temperature or 1 h at 100 °C). Finally, the PR was dissolved with acetone to release the carrier film/foil.

Conflict of Interest: The authors declare no competing financial interest.

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